CLAIMS

1. A vertical power transistor trench-gate semiconductor device comprising a semiconductor body having an active area with a plurality of electrically parallel transistor cells, wherein trench-gates in the active area each comprise a trench extending into the semiconductor body with gate material in the trench, wherein the transistor cells have source and drain regions of a first conductivity type which are separated by a channel-accommodating region of a second, opposite, conductivity type adjacent a trench-gate, wherein ruggedness regions are provided which are localised regions of the second conductivity type but which are more heavily doped than the channel-accommodating regions and which extend into the drain region, wherein the trench-gates are parallel stripes which each extend across the active area, wherein the source regions and the ruggedness regions extend to a source contact surface of the semiconductor body as alternating stripe areas having a width perpendicular to and fully between each two adjacent parallel stripe trench-gates, and wherein the device is characterised by the ruggedness regions being more heavily doped than the source regions.

2. A power transistor device as claimed in claim 1, wherein the cell pitch, that is the width of the source and ruggedness region stripes (mesa width) plus the width of an adjacent trench-gate stripe, is less than 2μm, and wherein the length of the source region stripes is in the range 10μm to 50μm.

3. A power transistor device as claimed in claim 2, wherein the cell pitch is in the range of 0.5μm to 1.5μm.

4. A power transistor device as claimed in claim 2 or claim 3, wherein the mesa width is approximately equal to the trench-gate stripe width.

5. A power transistor device as claimed in any one of claims 2 to 4,

wherein the length of the source region stripes is in the range 10μm to 30μm.

6. A power transistor device as claimed in claim 5, wherein the length of the source region stripes is approximately 20μm.

7. A power transistor device as claimed in any one of claims 2 to 6, wherein the length of the ruggedness region stripes is not greater than about 1μm.

8. A power transistor device as claimed in any one of claims 2 to 7, wherein the ratio of the length of the source region stripes to the length of the ruggedness region stripes is in the range 10 to 30.

9. A power transistor device as claimed in claim 8, wherein the ratio of the source region stripe length to ruggedness region stripe length is about 20.

10. A power transistor device as claimed in any one of claims 1 to 9, wherein the semiconductor body is silicon, wherein the ruggedness regions have p-type conductivity with a doping concentration in the range 10^{19} cm^{-3} to 10^{22} cm^{-3}, and wherein the source regions have n-type conductivity with a doping concentration in the range 10^{18} cm^{-3} to 10^{21} cm^{-3}.

11. A power transistor device as claimed in any one of claims 1 to 10, wherein the doping concentration of the ruggedness regions is approximately 10 times greater than the doping concentration of the source regions.

12. A power transistor device as claimed in claim 11, wherein the doping concentration of the ruggedness regions is about 10^{21} cm^{-3} and the doping concentration of the source regions is about 10^{20} cm^{-3}.

13. A power transistor device as claimed in any one of claims 1 to 12, wherein the ruggedness regions extend further into the drain region than the trench-gates.

14. A power transistor device as claimed in any one of claims 1 to 13, wherein the drain-source breakdown voltage of the device is in the range up to about 50 volts.